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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/611,919	07/03/2003	Erwin Hemming	47092.00032	5610

32294 7590 08/04/2005

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EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 08/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/611,919	HEMMING, ERWIN	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,15 and 16* is/are rejected.

7)☒ Claim(s) *12-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/17/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-5, 8 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Yeivin et al. (hereinafter Yeivin) US Patent 6,473,808 B1.

As for claims 1, 8 and 16, Yeivin teaches an interleaving method (and apparatus) for performing parallel access in a linear and interleaved order to a predetermined number of stored data samples, said method (and apparatus) comprising the steps of:

a) storing data samples in a memory array comprising a plurality of memory devices (memory array, Fig. 10, element 718);

b) using a first portion of an address of said memory array to address said memory devices (col. 14, lines 58-63 – an address word consisting of 15 bits uses 11 of the 15 bits to define which data word within a 2 k word to access);

c) using a second portion of said address to select at least one memory device to be accessed (col. 14, lines 58-63 – 4 bits of the 15 bits are used to select a memory bank within the memory array); and

d) changing a position of said first portion and said second portion within said address, when an access order is changed between a linear order and an interleaved order (col. 14, lines 58-63 – The interleaving can be done by swapping the least and most significant bits of the address word). Referring to Fig. 10, the memory selector (element 712) works in concert with the data mux and address mux (elements 716 and 714 respectively) to help form the 15-bit address word that is used to address the memory elements in the memory array. Per col. 14 lines 54-58, before switching to interleaving mode (memory addressing is now in linear mode), the four least significant bits are used to address the memory bank within the array. If however, the banks are to be addressed in interleaving mode, the same four bits used to address the memory banks within the array are sent to the most significant bits of the address bus (col. 14, lines 59-63).

As for claim 2, Yeivin teaches method according to claim 1, further comprising the step of performing a parallel access in a multiplexed manner using said second portion of said address portion as a multiplexing index (Fig. 10, elements 716 and 714 illustrate the data and address multiplexers respectively. Col. 14, lines 58-63 – An example is described where the 4 bits used to define the memory bank are sent to the address bus of the memory selector, which is fed to the multiplexer. The least significant bits comprise the "second portion" of the address as Yeivin's system is being used in interleaved mode).

As for claim 3, Yeivin teaches the method claim 1, wherein said second portion of said address corresponds to a predetermined number of most significant bits

of said address during a linear access order, and corresponds to a predetermined number of least significant bits of said address during an interleaved access order (Col.14, lines 58-63, in interleaved mode , the address and bank identification portions correspond to the most significant bits (first portion) and least significant bits (second portion) respectively. Again, interleaving was achieved by swapping the first and second portions of the address (col. 14, lines 52-53)).

As for claim 4, Yeivin teaches the method of claim 3, wherein said first portion of said address corresponds to a remaining number of bits within said address (col. 14, lines 58-63).

As for claim 5, Yeivin teaches the method according to claim 1, further comprising the step of subjecting said first portion of said address to an interleaving processing during an interleaved access order (col. 14, lines 52-53 – Interleave memory access is achieved when the first portion (most significant bits) of the address are used to define which data word is to be accessed. Those data are then sent to the address mux during interleave mode).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yeivin in further view Seo (US PG Publication 2003/0018942 A1).

Though Yeivin teaches all of the limitations of claim 1, he fails to specifically include the first portion of the address as comprising ten address bits, and the second portion as comprising two address bits. The example provided in col. 14, lines 48-64 is only one example of many possibilities for his system which includes 11 bits for the first portion, and 4 bits for the second. Seo teaches a common memory device and controlling method, which does in fact address four memory devices within an array using two bits, however his system only uses 8 bits for the first portion (actual word address) – Paragraph 0044, lines 1-5. It would have been obvious to one of ordinary skill in the art at the time of the invention for Yeivin to further include other possible address sizes (such as for Seo's example, or ten bits in the first portion, and two in the second to address four memories within the array as another example) in his system. The example provided in Yeivin's teachings is merely an arbitrary example to illustrate how his system works to address the memory within the array.

3. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yeivin in further view Schmidt (US PG Publication 2002/0128037 A1).

Though Yeivin teaches all of the limitation of claim 8, he fails to include his apparatus as one integrated system on a single chip device. Schmidt however

teaches a single chip wireless communication integrated circuit (Fig. 1, paragraph 0014, lines 1-12). It would have been obvious to one of ordinary skill in the art at the time of the invention for Yeivin to further integrate his high performance communication controller on a single chip device. By doing so, Yeivin would benefit from increased performance, and lower communication overhead as taught by Schmidt (paragraph 0008, lines 1-11).

4. Claims 7 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeivin in further view of Merritt et al. (hereinafter Merritt) US PG Publication 2003/0063502 A1.

As for claims 7 and 11, though Yeivin teaches all of the limitations of claims 1 and 8, he fails to teach generating a first portion of the address by an address counting function. Merritt does however teach a distributed write data driver system for burst access memories, which allows for either interleaved or sequential access of a memory following a single column address command (paragraph 0011, lines 1-15). The address counter is advanced on the rising edge of the control signal /CAS and the generated address is presented to the memory array on the falling edge (paragraph 0035, lines 21-29). It would have been obvious to one of ordinary skill in the art at the time of the invention for Yeivin to utilize Merritt's address counter for address generation. By doing so, Yeivin's system would benefit from internal address incrementing, which in turn would allow read/write commands to the memory to be

issued only once per burst access which eliminates the need to toggle the control line at high speeds (Merritt, paragraph 0011, lines 1-12).

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yeivin in further view of Suzuki et al. (hereinafter Suzuki) US PG Publication 2003/0225985 A1.

Though Yeivin teaches all of the limitations of claim 8, he fails to specially teach the use of single-port RAM devices. Suzuki however teaches an interleaver for iterative decoders, which specifically uses single-port RAM devices. Though Suzuki briefly discusses the benefits of a dual-port memory for interleaver decoders, his invention teaches the use of single port memory (paragraph 0014, lines 1-15). It would have been obvious to one of ordinary skill in the art at the time of the invention for Yeivin to further include single-port memory devices in his memory array. By doing so his system would benefit from memory modules that are far more cost effective than dual port memory structures (paragraph 0012, lines 1-7).

6. Claims 8 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiu et al. (hereinafter Shiu) US Patent 6,392,572 B1 in further view of Yeivin.

Though Shui teaches a buffer architecture for a turbo decoder comprising a turbo interleaver, he fails to specifically teach an apparatus as described in claim 8 of applicant's disclosure. Yeivin however teaches all of the limitations of claim 8 in his high performance communication system (as described above). It

would have been obvious to one of ordinary skill in art at the time of the invention for Shiu to further include Yeivin's high performance communication system for turbo decoding. Do doing so, Shui's system would benefit by including the ability of handling high-speed data streams associated with a variety of communication protocols as taugh by Yeivin (col. 4, lines 37-41).

Allowable Subject Matter

7. Claims 12-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As for claim 12, though the combined teachings of Yeivin and Merritt meet all the limitations of claim 11, their teachings fail to further limit the apparatus to convert the output address of the address counter according to a predetermined interleaving scheme.

As for claim 14, though Yeivin and Merritt's combined teachings meet the limiations set forth in claim 8, they fail to further limit the apparatus by using a control switch for switching the first and second portions of the address in response to an access order selection signal.

Claim 13 further limits claim 12 therefore it is deemed allowable.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Van Lunteren (US Patent 6,453,380 B1) teaches address mapping system for configurable memory.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

CEW

Reginald G. Bragdon
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PRIMARY EXAMINER